

Appl. No. 09/727,032  
Amdt. dated June 23, 2004  
Reply to Office action of April 15, 2004

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A computer system, comprising:  
an internal computer bus coupling together a plurality of bus devices, wherein each of said plurality of bus devices includes a queue in which pending operations awaiting execution onto the bus are stored while the bus device awaits access to the computer bus; a bus arbiter coupled to the computer bus, said bus arbiter receiving requests from said plurality of bus devices to obtain access to the computer bus and wherein each of said bus devices transmits a signal to said bus arbiter indicating a number of operations pending in the queue of the bus device; wherein said bus arbiter resolves conflicting requests from said bus devices based on the number of operations pending in the queue of the bus devices requesting bus access.
2. (Cancelled).
3. (Cancelled).
4. (Cancelled).
5. (Previously presented) The system of claim 1, wherein said bus arbiter compares the signals indicating the number of operations pending in the queue from any bus devices requesting access to the computer bus, and awards access to the bus device with the most operations pending in its associated queue.

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6. (Original) The system of claim 5, wherein said bus arbiter breaks any ties between bus devices with an equal number of operations pending in the queue based on a predetermined priority value assigned to each bus device.

7. (Previously presented) The system of claim 5, wherein said bus arbiter breaks any ties between bus devices with an equal number of operations pending in the queue based on which device was last granted access.

8. (Original) The system of claim 5, wherein the signal indicating the number of operations pending in the queue comprises a multi-bit signal.

9. (Original) The system of claim 8, wherein the multi-bit signal comprises  $n$  bits, with  $2^n$  = number of entries in the queue of each device.

10. (Previously presented) The system of claim 1, wherein the bus device access request indicates the number of operations pending in the queue of the bus device through a combination of specific numbers and at least one range value.

11. (Currently amended) A computer system, comprising:  
an internal bus;  
a plurality of bus devices, each of which couples to said bus, and each of which is capable of running cycles on said bus, and each of said bus devices includes a queue in which pending operations pending transmission onto said internal bus are stored while the bus device awaits access to the bus;  
a bus arbiter coupled to the bus, said bus arbiter receiving request signals from said plurality of bus devices that are seeking to run a cycle on said bus;  
wherein any of said devices that include one or more operations in its queue transmits the request signal to said bus arbiter requesting

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access to said bus and indicating a number of operations pending in its associated queue;

and wherein said bus arbiter resolves conflicting requests from said bus devices based on the number of operations pending in the queues of the requesting devices.

12. (Previously presented) The system of claim 11, wherein each of said plurality of bus devices is capable of running bus cycles on said bus as a master device.

13. (Previously presented) The system of claim 11, wherein the request signal comprises a sideband signal between the bus devices and the bus arbiter.

14. (Previously presented) The system of claim 13, wherein the queue associated with each bus device has the same number of entries.

15. (Original) The system of claim 13, wherein at least two of said bus devices have queues with a different number of entries.

16. (Cancelled).

17. (Previously presented) The method of claim 18, wherein the act of determining if more than one bus device has requested access includes monitoring for a request signal from each of the bus devices capable of initiating cycles on the computer bus.

18. (Currently amended) A method of resolving conflicting bus access requests in an internal computer bus, comprising the acts of:

determining if more than one bus device has requested access to the internal computer bus;

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determining workload associated with each bus device requesting access to the internal computer bus; and  
granting access to the bus device that has the greatest workload;  
and wherein the act of determining the workload associated with each bus device includes receiving a signal from each device indicating a number of operations awaiting ~~execution in that device~~ transmission onto said bus.

19. (Original) The method of claim 18, wherein the number of operations awaiting execution is determined based on the number of operations pending in a queue in that device.

20. (Previously presented) The system of claim 18, further comprising an act of breaking any ties between devices with equal workloads based on other priority criteria.